CHARGE BURSTS THROUGH DIELECTRIC LAYERS OF 4H-SIC/SiO_2 METAL OXIDE SEMICONDUCTOR CAPACITORS

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ABSTRACT

Small bursts of inversion layer charge in 4H-SiC metal oxide semiconductor capacitors leak through the oxide layer leading to discontinuities during capacitance-time measurements. This behavior has been observed using non-equilibrium capacitance-time (*C-t*) and current-time (*I-t*) measurements, at room temperature and at 400 °C.

INTRODUCTION

Silicon carbide is a unique compound semiconductor because, in addition to being ideally suited for high temperatures, extreme environments, and high power devices, it has the same native oxide as silicon – silicon dioxide. Consequently, intense research has been pursued toward developing a commercially viable SiC MOSFET, as it would offer better performance than its silicon counterpart in many situations. Although problems still exist, it is reasonable to predict that a SiC MOSFET will become commercially available in the near future. For this reason, reliability of SiC MOSFETs is becoming an important concern [1].

Many of SiC's useful properties are due to its wide band gap. Paradoxically, the wide band gap also causes a major reliability concern for the dielectric, since it necessitates substantially smaller oxide-semiconductor energy barriers than those of the standard Si/SiO_2 system. Thus, dielectric breakdown has been found to be worse for SiC/SiO_2, both by time-zero [2] and time-dependent breakdown [3] methods. In addition, the oxide tunneling current is higher than that in silicon [4], and is worse at high temperatures [5]. Furthermore, it has been found that SiC/SiO_2 devices suffer from negative bias temperature instability (NBTI), which is also a major reliability issue for silicon devices [6]. Reliability troubles at elevated temperatures are especially concerning, as SiC is desirable for its high temperature properties.

In the following work, we present evidence which suggests that sudden bursts of inversion charge drift through the dielectric layer of 4H-SiC/SiO_2 MOS capacitors (MOS-C), without causing destructive breakdown. Evidence consistent with this theory is present in the time-dependent capacitance (*C-t*) and current (*I-t*) behavior, at room temperature and at 400 °C. To the best of the authors' knowledge, this behavior has not been previously reported in either SiC/SiO_2 or Si/SiO_2 MOS capacitors.

EXPERIMENTAL

MOS capacitors (MOS-C) were formed from n-type 4H-SiC samples, grown with Dow Corning chlorosilane/propane chemistry. The 20 µm epitaxial layers were nitrogen doped to an approximate concentration of 10^{16} cm^{-3}. A 45 nm SiO_2 layer was grown thermally, and passivated with NO. Gates were formed from contacts of approximate diameters 377 and 675 µm, patterned using photolithography. The devices were measured in an electrically isolated probe station with a maximum temperature of 400 °C.

The fundamental purpose of our work is to characterize carrier generation lifetime (τ_g) of 4H-SiC epitaxial layers using the pulsed MOS-C technique, which is detailed in [7]. The basic procedure starts with an MOS capacitor in accumulation (V_G = 5 V); and the gate voltage is switched to an inversion bias level (V_G = -10 V). The inversion layer does not form immediately, since minority carriers must be thermally generated. Thus, as the inversion layer forms, the space charge region (scr) width below the gate decreases and the capacitance increases. The speed and behavior of this recovery contain information about the generation lifetime in the scr of the device. The MOS-C recovery time depends on the generation rate, which is proportional to the intrinsic concentration, n_i. At room temperature, n_i in 4H-SiC is about 500 cm^{-3} and the generation rate is negligible. Thus we use the probe station's maximum temperature of 400 °C, which brings n_i to about 10^8 cm^{-3}, and reduces the pulsed MOS-C recovery time to several minutes.

RESULTS AND DISCUSSION

It was observed that some of our SiC MOS capacitors have a discontinuity in the *C-t* curve (Fig. 1). The proposed explanation for this behavior is the following: during the recovery from deep depletion, inversion charge slowly builds up at the oxide-semiconductor interface. The electric field across the oxide continually increases, due to the increasing inversion and gate charge. The oxide electric field of the device in inversion (V_G= -10 V) is about 2 MV/cm. At points (a) and (b) in Fig. 1, a local instantaneous breakdown occurs, which allows some of the inversion charge to drift through the dielectric. However, this is not a destructive breakdown because after the burst, the inversion layer continues to form until complete inversion is reached. The amount of charge which escapes through the oxide is proportional to the size of the capacitance drop – thus it is higher for point (a) on Fig. 1 than point (b). This makes sense qualitatively, as the electric field is higher at point (b) than at point (a).

Using the same concepts and biasing sequence as the pulsed MOS-C method, time-dependent current measurements were made. The devices are quickly switched from accumulation to inversion biases, resulting in a current which depends on the scr width. As the inversion layer forms, the width of the scr shrinks, and the current drops. Once the full inversion layer is formed and the ideal device is in equilibrium, the current ceases. During this process, sometimes a discontinuity occurs (Fig. 2) which is consistent with that observed in the *C-t* behavior of Fig. 1. Again, when the inversion charge is lost, the scr becomes wider than before. In Fig. 2, this scr widening manifests itself as a higher current, which is caused by the larger volume of carrier generation.

A final experiment uses the fact that the room temperature generation rate is negligible in 4H-SiC. Thus, if we use a light source to introduce generation to form an inversion layer, once the source is removed and the device settles to equilibrium it should ideally have a constant capacitance. However, if inversion charge is lost through the oxide, the capacitance will decrease to reflect the

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resulting increase in scr width [9]. A sample plot is given in Fig. 3, which has discontinuities that indicate, as seen previously, that charge has escaped through the oxide. This case is especially interesting because it shows that the behavior is present even at room temperature.

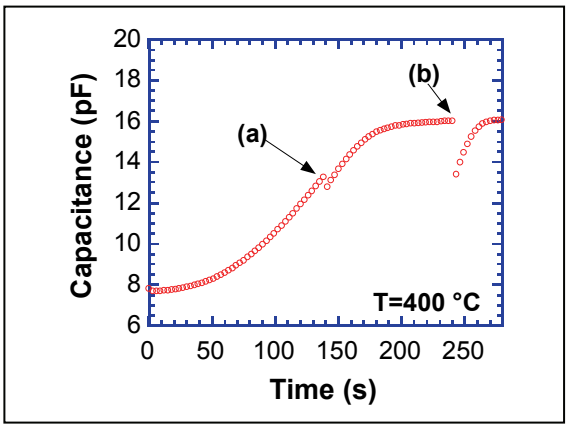

FIGURE 1. CAPACITANCE VERSUS TIME WITH THE DISCONTINUITIES INDICATING A BURST OF CHARGE THROUGH THE GATE OXIDE.

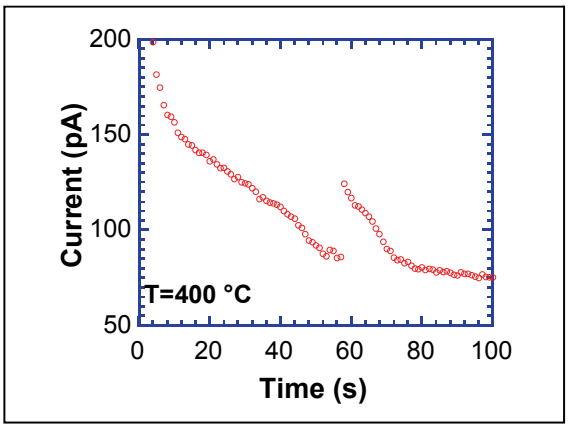

FIGURE 2. CURRENT VERSUS TIME WITH THE DISCONTINUITIES INDICATING A BURST OF CURRENT THROUGH THE GATE OXIDE.

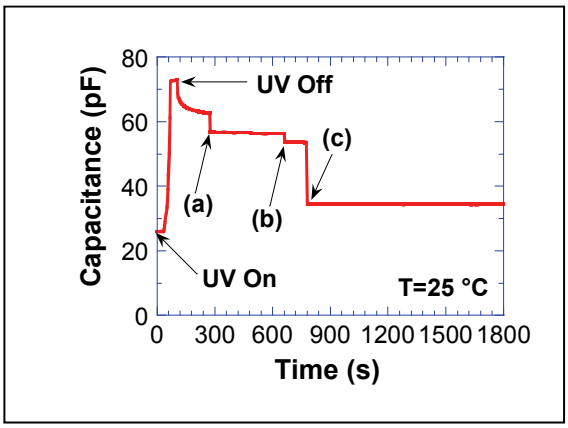

FIGURE 3. CAPACITANCE VERSUS TIME WHICH BEGINS WITH THE DEVICE IN INVERSION. THE DISCONTINUITIES INDICATE A BURST OF CURRENT THROUGH THE GATE OXIDE.

It is not known whether this behavior is due to oxide or material related defects – or a combination of the two. Charge bursts are not present in all devices, and usually occur at oxide fields higher than 1 MV/cm. This phenomenon could potentially impact the reliability of SiC MOSFETs, as well as non-volatile memory devices. In a MOSFET, this behavior might manifest itself as a sudden, temporary decrease in current; the entire event would be much faster since the lost carriers would quickly be restored by the source. In a non-volatile memory element, the effect would be to change the state of the device, since the presence of an inversion layer generally indicates whether the device is in the "1" or "0" memory state.

CONCLUSION

A unique phenomenon has been experimentally observed in which discontinuities appear in the time dependent capacitance and current behavior of 4H-SiC/SiO_2 MOS capacitors. The proposed explanation is that a fraction of inversion charge bursts through the oxide layer of a 4H-SiC/SiO_2 MOS-C. To the best of the authors' knowledge, a similar behavior has not been previously observed in either Si/SiO_2 or SiC/SiO_2 MOS capacitors of any type.

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