Evidence of negative bias temperature instability in 4*H*-SiC metal oxide semiconductor capacitors

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Generation lifetimes and interface state densities of *n*-type 4*H*-SiC metal oxide semiconductor (MOS) capacitors are characterized by using the pulsed MOS capacitor technique. A decrease in lifetime and increase in interface state density occurs when the devices are negatively biased at 400 °C. This behavior is consistent with an effect seen in Si/SiO_2 devices known as negative bias temperature instability. A portion of the lifetime degradation caused by this effect can be recovered by removing the negative bias as well as by positively biasing the device. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2748327]

It is well known that silicon carbide has many desirable properties. One of the most important of these is its ability to operate at high temperatures. Due to its wide band gap (3.265 eV for 4*H*),[1] SiC can operate at temperatures in excess of 600 °C.[2] Furthermore, the fact that its natural oxide is SiO_2 creates a potential for use of SiC in metal oxide semiconductor (MOS) devices. However, this major advantage of SiC also subjects it to some of the same challenges faced by the silicon industry. The most widely recognized challenge has been creating a high quality SiO_2/SiC interface with an acceptable interface state density (D_{it}).[3–6] Another important challenge, which has gained a great deal of attention in the *silicon* industry in recent years, is negative bias temperature instability (NBTI).[7] That raises the question whether NBTI also occurs in SiC.

NBTI in silicon metal oxide semiconductor field effect transistors (MOSFETs) causes a negative threshold voltage shift, degrades channel mobility, and reduces drain current. The effects of NBTI are also present in MOS capacitors (MOS-Cs), resulting in a reduced generation lifetime and an increased interface state density.[8] It is generally accepted that NBTI is the result of interface and oxide trap generation.[9–11] The proposed mechanism for these effects in Si is not fully understood; the most recent views are discussed by Schroder and Babcock.[7] However, it is generally believed that the effect requires negative gate voltage and holes in the semiconductor and is accelerated by high temperatures.

Although little work has been done explicitly on NBTI effects in SiC,[12] there is no reason to believe that the SiO_2/SiC interface is immune to this effect. Furthermore, the ensuing D_{it} increase associated with NBTI could be especially detrimental to *p*-MOSFET mobility, especially if high temperature operation is desired. This letter discusses an anomaly observed when characterizing *n*-type 4*H*-SiC MOS capacitors, which we believe to be the result of NBTI degradation.

4*H*-SiC *n*-type samples with an epitaxial layer thickness of 20 μm and a doping concentration of 10^{16} cm^{-3} grown by Dow Corning were used in the present experiments. The oxidation procedure began with a four part preparation process consisting of an organic clean, a buffered HF etch (6:1), and a heavy metal clean using $H_2SO_4:H_2O_2$ (1:1), followed by $NH_3OH:H_2O_2:DIW$ (3:3:10) and $HCl:H_2O_2:DIW$ (3:3:10). The final step was a deionized water (DIW) rinse/buffered HF dip/DIW rinse. The oxidation furnace was flushed with oxygen for 15 min and 500 SCCM (SCCM denotes cubic centimeter per minute at STP) before the samples were loaded at 900 °C. The furnace temperature was then ramped to 1150 °C at 5 °C/min and held at this temperature for a 4 h oxidation. The samples were then held in flowing Ar for 30 min, after which the furnace was ramped to 1175 °C (5 °C/min) for a 2 h passivation using pure NO (nitric oxide). Following passivation, the samples were ramped back to 900 °C in Ar at 5 °C/min and removed from the furnace. Circular contacts of diameters of 377 and 675 μm were patterned using photolithography. Molybdenum gate contacts with gold overlayers (each ~150 nm) were sputtered in Ar. The contacts were defined by lift-off using acetone. The oxide thickness was about 45 nm.

The capacitance and conductance were measured with an Agilent 4294A impedance meter with a source frequency of 100 kHz. The meter was connected to an electrically isolated probe station capable of measurements at temperatures up to 400 °C. Test sequences were programed in Agilent's Instrument BASIC. Dry N_2 flowed over the sample's surface during measurements to minimize mobile surface charging effects. The following measurement sequence is based on the pulsed MOS capacitor technique of measuring generation lifetime. The theory is described in detail elsewhere.[13] First, the gate voltage was swept from accumulation (V_G=7 V) to deep depletion (V_G=−10 V) at a 250 mV/s sweep rate to obtain base line capacitance-voltage (*C*-*V*) and conductance-voltage (*G*-*V*) curves. Even at 400 °C, an exceedingly slow sweep rate is required to form an inversion layer in 4*H*-SiC,

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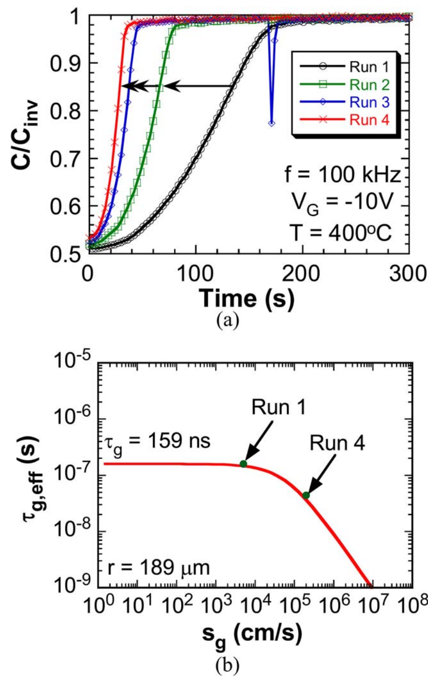

FIG. 1. (Color online) (a) *C-t* results from test described in text. Part (b) illustrates a plot of $\tau_{g,\mathrm{eff}}$ vs s_g to indicate the possible locations of the effective lifetimes obtained in part (a) if increased surface generation is responsible for the increase in lifetime.

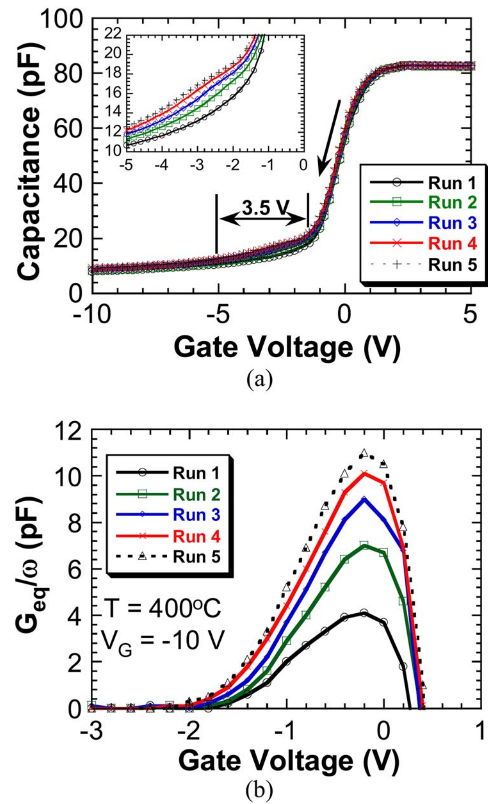

FIG. 2. (Color online) (a) *C-V* results from test sequence described in the text with a closer view of the "bulge" created by interface state generation in the inset, and (b) the corresponding equivalent parallel conductance. $T = 400$ °C and $V_{\mathrm{G}} = -10$ V.

thus all *C-V* measurements are assumed to enter deep depletion. Immediately following this measurement, the gate is biased for approximately 1 s into accumulation, and then pulsed in deep depletion for 10 min while an inversion layer forms. During this time, a capacitance-time (*C-t*) curve is recorded, giving an effective generation lifetime $\tau_{g,\mathrm{eff}}$ and effective surface generation velocity $s_{g,\mathrm{eff}}$. After the pulsed MOS-C measurements, the *C-V*/*G-V* measurements are made. This sequence is repeated four times.

The normalized data of the four consecutive *C-t* measurements are shown in Fig. 1(a). Each successive curve recovers faster than the previous one, indicating that the lifetime is shorter after each pulsed MOS-C measurement. The MOS-C recovery time depends on interface or bulk space-charge region electron-hole pair generation. We do not believe that these pulsed measurements alter the bulk generation rate but rather alter interface state generation. A known symptom of NBTI in the SiO_2/Si system is that D_{it} increases with time for negatively biased MOS devices, especially when at an elevated temperature. This decrease in lifetime is exactly what is seen in the Zerbst plots (not shown); $\tau_{g,\mathrm{eff}}$ drops from 159 to 44 ns. Furthermore, an increase in $s_{g,\mathrm{eff}}$ from 77 to 535 cm/s is observed.

If NBTI is truly the cause of this decrease in lifetime, then the only component of $\tau_{g,\mathrm{eff}}$ which should have changed is the surface generation velocity. Thus, it is useful to consider the relationship between the true value of the surface generation velocity s_g and the effective lifetime $\tau_{g,\mathrm{eff}}$ obtained from the Zerbst plot. The two are related by $\tau_{g,\mathrm{eff}} = \tau_g / 1 + 2 s_g \tau_g / r$, where r is the device radius and s_g and τ_g the surface generation velocity and bulk generation lifetime, respectively. Figure 1(b) gives a plot of this equation using a bulk lifetime of 159 ns, with an estimation of where the first and final points should be on the curve if the change in $\tau_{g,\mathrm{eff}}$ is only due to the creation of interface states. The curve is insensitive to s_g at low values and we can only say that $s_g \leq 2000$ cm/s for the initial value which increases to $\sim 2 \times 10^5$ cm/s after bias stress. If the effective lifetime decrease is due to an increased D_{it} which increases s_g, then this behavior is analogous to NBTI in silicon.

The *C-V* and *G-V* data show that the interface state density has increased after each pulsed MOS measurement. The *C-V* curves in Fig. 2(a) show a stretching out in the deep depletion regime, which can be attributed to higher D_{it}. This interface "stretch out" becomes more significant with each measurement, indicating that more interface states are generated. To first order, the interface state density is estimated by the flatband voltage shift as $N_{\mathrm{it}} \approx \Delta V_{\mathrm{FB}} C_{\mathrm{ox}} / q = 1.6 \times 10^{12}$ cm^{-2}. As noted by Nicollian and Goetzberger, the equivalent parallel conductance is more sensitive than the capacitance to changes in interface state density.[14] Thus, it is expected that a significant increase in the conductance occurs during the test sequence, which is exactly the behavior depicted by the corresponding *G-V* results in Fig. 2(b).

NBTI is generally considered to be caused by holes.[7] In order to determine if holes are important, we performed a similar test sequence on the same device at a temperature of 200 °C. At this temperature, the intrinsic concentration n_i in 4*H*-SiC is only about 500 cm^{-3}, and electron-hole pair generation is negligible within the measurement time. Thus, we can assume that very few holes are generated, and the device remains depleted. On the other hand, 200 °C is high enough to cause the NBTI effect to occur in a silicon MOS-C (if holes are present).

The significant range of the second set of *C-V* measurements is shown in Fig. 3(a). Although a flatband voltage shift

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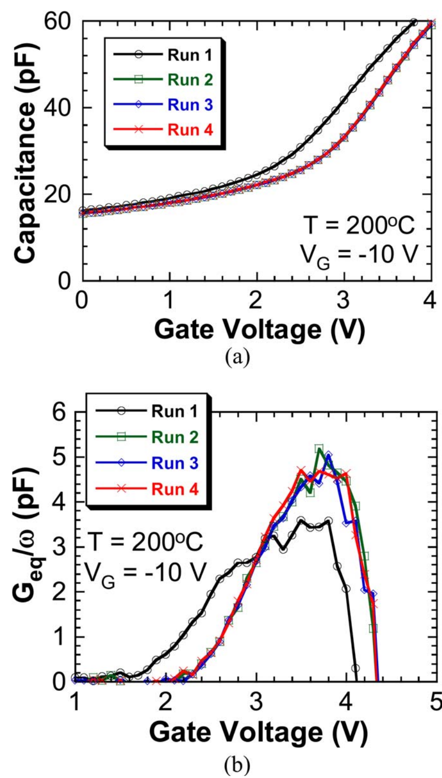

FIG. 3. (Color online) (a) Relevant portion of the *C-V* results and (b) corresponding *G-V* curves obtained from the 200 °C test described in the text. The NBTI effect is not apparent in these results.

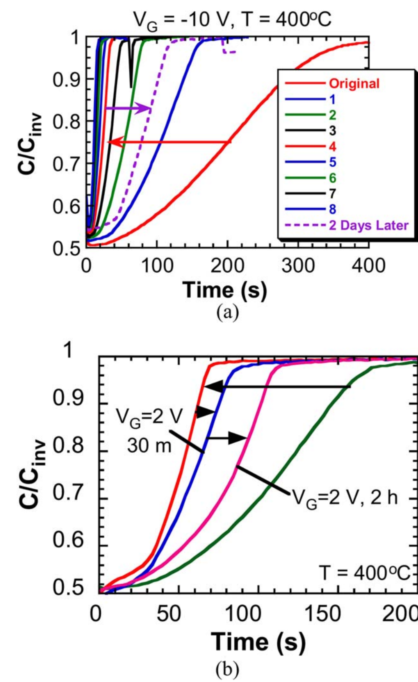

FIG. 4. (Color online) (a) *C-t* data showing a progressive recovery time reduction. The dashed line is after two days of inactivity. (b) *C-t* data for stressing the device with a positive gate voltage subsequent to the onset of NBTI. The rightmost curve is the original, the leftmost is after a long negative stress, and the two center curves after periods of positive bias.

is present, the stretch out of Fig. 2(a) is not observed. We attribute this flatband shift to the mobile ion movement. Furthermore, the corresponding *G-V* plot in Fig. 3(b) shows very little change in the peak or spread of the conductance. Thus, it can be concluded that negligible interface state generation occurred during the 200 °C test sequence, which is consistent with the fact that NBTI requires holes.

An interesting property of NBTI in Si is that the effect will partially or totally reverse itself once the negative bias is removed.[15,16] To determine if this recovery is present in SiC, we show in Fig. 4(a) the results of ten consecutive pulsed MOS data and a measurement made two days later, with the device remaining unbiased for those two days. As expected, the recovery transient continually decreased during the series of measurements, indicating that NBTI was active. When the device was retested after a two day period of inactivity, the recovery time had increased significantly, indicating that some of the interface states have been repaired. We extended the "healing" portion by applying a *positive* gate bias, shown in Fig. 4(b). First, the device was biased for 2 h in inversion ($V_G = -10$ V) at 400 °C. Next, it is biased to $V_G = 2$ V for 30 min and a *C-t* scan is taken. This was followed by an additional 2 h at $V_G = 2$ V and a final *C-t* measurement. As observed previously, the recovery time decreases significantly subsequent to the negative bias, but then increases with each positive bias step. It can therefore be concluded that significant recovery does occur during the positive bias.

In summary, evidence of NBTI in *n*-type 4*H*-SiC MOS capacitors has been presented. The decreased effective lifetime demonstrated by *C-t* measurements and increased interface state density indicated in the *C-V* and *G-V* tests are consistent with the known properties of NBTI in Si. The increased D_{it} can be partially recovered by removing the bias or applying a positive gate voltage. This effect must be considered when making generation lifetime measurements in *n*-type SiC material using the pulsed MOS technique, as it will cause lifetimes to appear artificially short.

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